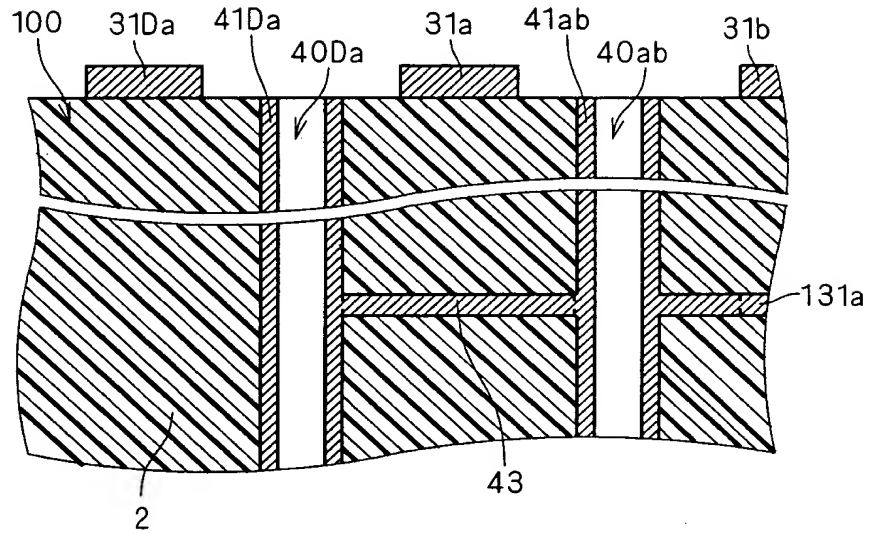
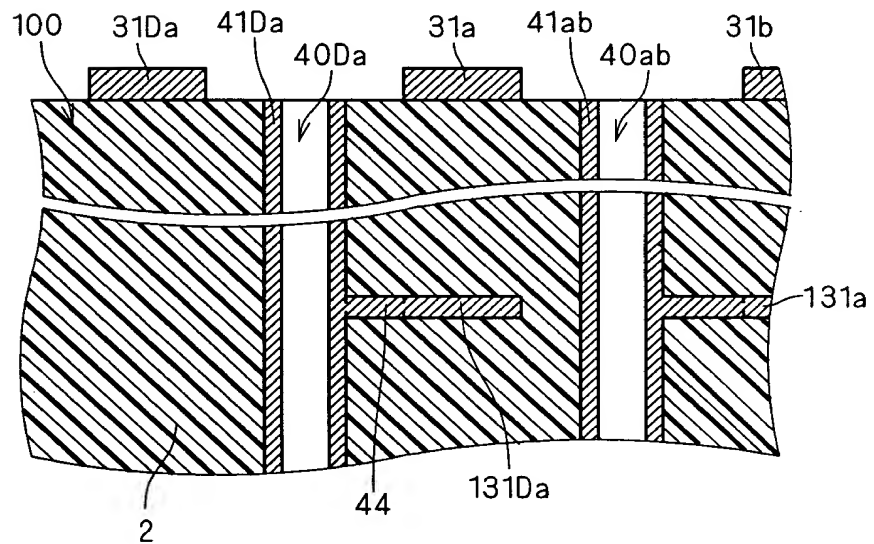




F I G . 5



F I G . 6





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FIG. 15 PRIOR ART

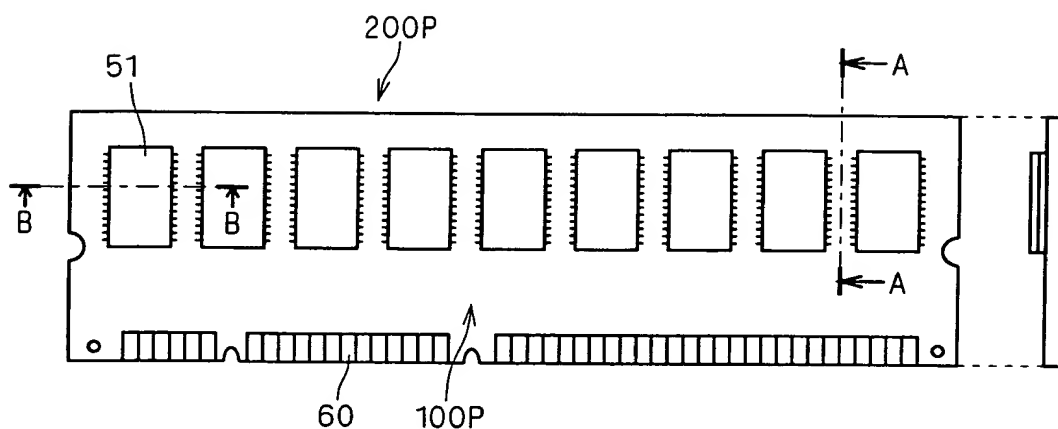
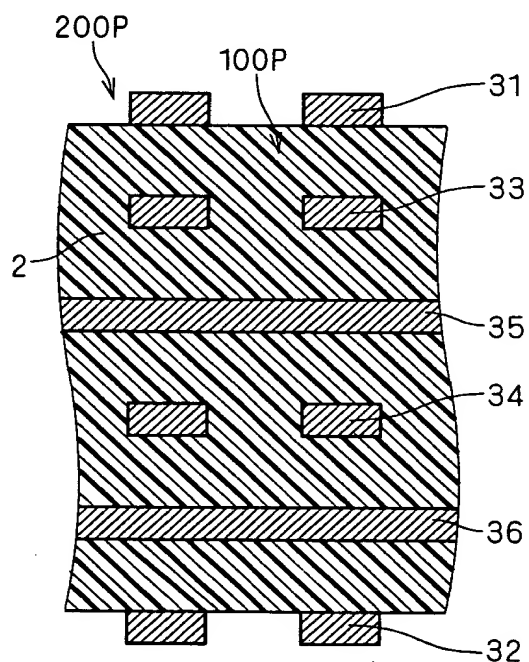


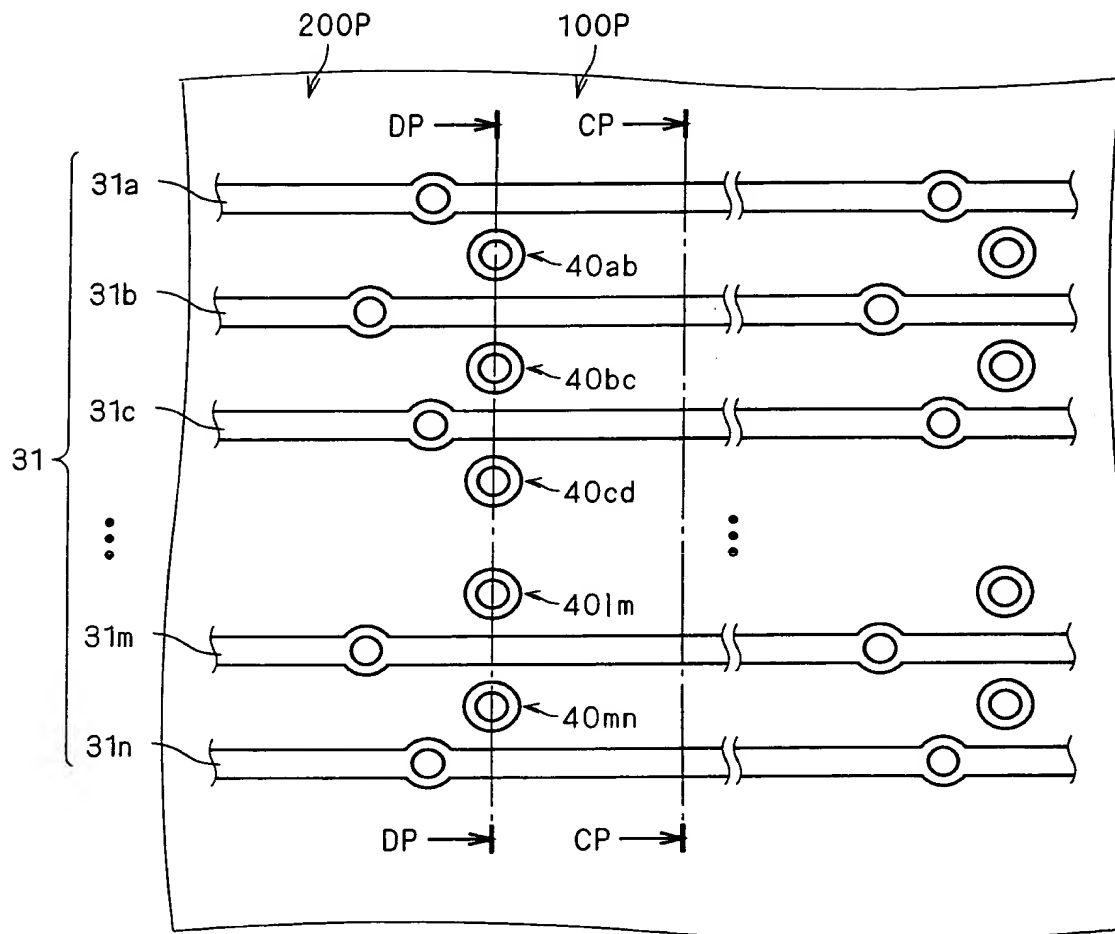
FIG. 16 PRIOR ART





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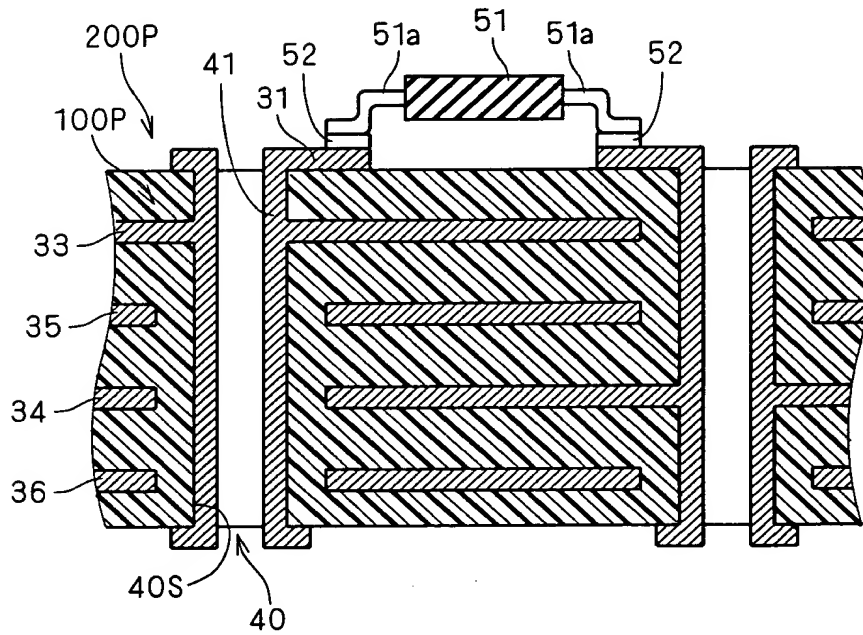
**FIG. 17 PRIOR ART**



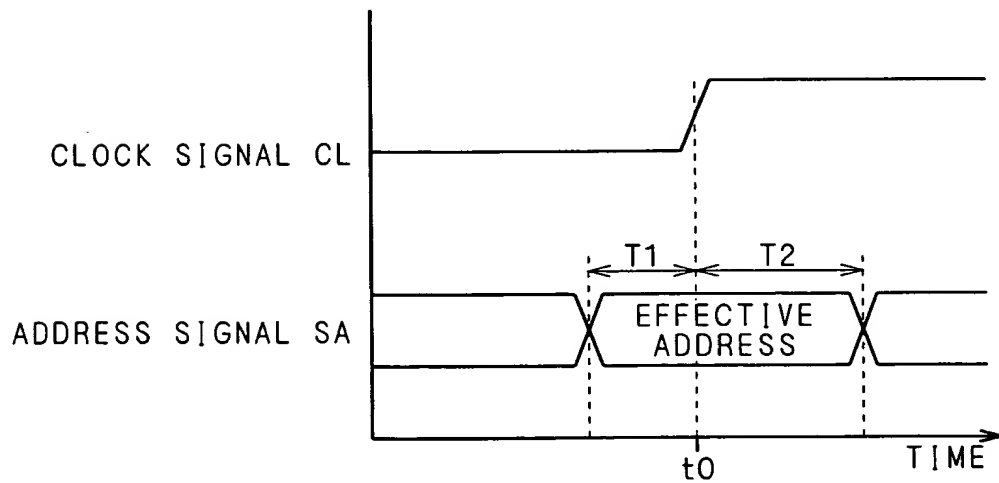


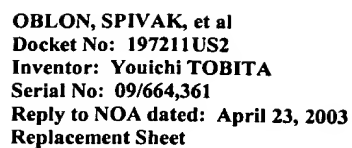
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**F I G . 18 PRIOR ART**



**F I G . 19 PRIOR ART**





The diagram shows a multi-stage resonant circuit 31. It starts with a series inductor 31a, followed by a parallel LC resonant circuit 40ab consisting of a series inductor 41ab and a capacitor 40ab. This is followed by a capacitor CST, then another series inductor 31b, another parallel LC resonant circuit 40bc with series inductor 41bc and capacitor 40bc, and another capacitor CST. This pattern repeats through an ellipsis to a final stage with series inductor 31n, parallel LC resonant circuit 40mn with series inductor 41mn and capacitor 40mn, and a final capacitor CST. The entire circuit is labeled 31 at the bottom.

The diagram shows three signals over time: CLOCK SIGNAL CL, ADDRESS SIGNAL SAa, SAn, and ADDRESS SIGNAL SAb ~ SAm. The clock signal CL transitions from low to high at time  $t_0$ . The address signals SAa, SAn and SAb ~ SAm are shown as pulses that are effective during a specific time window. The time interval between the falling edge of the clock and the start of the address pulse is  $\Delta t$ . The time interval between the rising edge of the clock and the end of the address pulse is  $T_3$ . The time interval between the falling edge of the clock and the start of the address pulse is  $\Delta t$ . The time interval between the rising edge of the clock and the end of the address pulse is  $T_3$ . The time interval between the falling edge of the clock and the start of the address pulse is  $\Delta t$ . The time interval between the rising edge of the clock and the end of the address pulse is  $T_3$ .